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Dated: April 4, 2002 Signature: _____ (Marcus J. Millet)

Docket No.: TESSERA 3.3-018
CONT CONT II DIV CONT CONT
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APR 08 2002
PATENT & TRADEMARK OFFICE 2800

#13
4/21/02

In re Patent Application of:
Khandros et al.

Application No.: 09/656,690 Group Art Unit: 2812

Filed: September 7, 2000 Examiner: D. Graybill

For: FACE-UP SEMICONDUCTOR CHIP ASSEMBLIES

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Commissioner for Patents
Washington, DC 20231

RESPONSE

Dear Sir:

The present communication is responsive to the Official Action mailed December 4, 2001. Said Official Action set a term of one month for response, which term was expressly made subject to extension under 37 CFR § 1.136(a). A petition for a three-month extension of the term for response to said Official Action, to and including April 4, 2002 is transmitted herewith.

APPLICATION OF COPIED CLAIMS TO DISCLOSURE -

Said Official Action indicated that the reply filed September 24, 2001 failed to specifically apply "each limitation or element of each of the copied claims to the disclosure of the application," and required applicant to further apply the claim elements discussed below.

Dielectric -

The limitation to a "dielectric" interposer in claim 1, paragraph (b) is applied to the specification as follows:

The specification teaches the use of a dielectric interposer as follows: "The chip assembly according to this aspect of the invention also includes a sheet-like dielectric element, referred to herein as 'interposer,' overlying the front surface of the chip" (p. 7, lns. 25-29); "a sheet-like dielectric interposer . . ." (p. 9, lns. 24-25); "assembling a sheet-like dielectric interposer to the chip" (p. 11, lns. 33-34); and "dielectric interposer 32" (p. 19, ln. 9), as well as "a sheet-like dielectric interposer 836." Manifestly, the "interposers" referred to at page 30, line 31 to page 31, line 19 are interposers in accordance with the other teachings of the specification quoted above. The same application of claim terms to the disclosure of the specification applies with respect to claim 18, paragraph (b), which also refers to "a dielectric interposer."

Elastomer -

The indication in the Official Action that the term "elastomer" has not been applied to the disclosure is not understood. With regard to claim 3, applicant had previously pointed out the step of positioning a "compliant layer" between the "top layer 838" of the interposer and the chip 820 (claim chart, section bridging pp. 7-8 of applicant's last previous response), and applicant had pointed out that the compliant layer 840 (Fig. 13) includes an elastomeric material. This is substantiated by the specification. "The compliant, low-modulus material of bottom layer 840 may be an elastomer. Desirably, the low-modulus material has elastic properties (including modulus of elasticity) comparable to those of soft rubber . . ." (p. 32, ln. 36 to p. 33, ln. 3). In that embodiment, the "top layer 838" of the "interposer 836" referred to in the specification meets the recitation of the "interposer" in claim 3; the compliant layer or elastomer 840 is positioned

between each chip and the "respective interposer on the chip." As also pointed out previously, the specification also contemplates providing the "compliant layer" or elastomer as a "separate compliant underlayer," which layer may be positioned "on the chip surface, before the top layer and the terminals are positioned on the compliant layer." The separate compliant underlayer may include an "elastomer" such as a "silicone elastomer" (p. 41, lns. 15-35). In short, the specification makes it plain that an elastomer bottom layer or underlayer may be assembled to the chip either before assembling the flexible top layer or interposer to the chip, or as a part of an assembly including both the top layer and the underlayer. Either arrangement meets the recitations of claim 3. The same comments apply with respect to application of the word "elastomer" in claims 9, 15, 20, 26 and 32 to the specification.

Any Side -

With respect to the recitation that one of the wires is oriented at an angle substantially less than 90 degrees from "any side" of the section of interposer, the only possible meaning of the recitation "less than 90 degrees" is that the bonding wire must be oriented at an angle other than 90 degrees to any side of the "section of interposer," *i.e.*, that the bonding wire is not perpendicular to any "side" of the "section" of the interposer. Merely by way of example, in *Razon et al.*, U.S. Patent 5,950,070 ("the '070 patent"), bonding wire 108a (Fig. 3) extends across one side or edge of interposer 106. The bonding wire defines one acute angle (less than 90 degrees) with that side and also defines one obtuse angle (greater than 90 degrees) with the same side. The recitation that the bonding wire must be oriented at an angle "substantially less than 90 degrees from any side" of the interposer section means that the bonding wire must not be perpendicular to any side of the

interposer. Applicant had previously pointed out (chart, p. 9 of applicant's last previous response) that in Fig. 13, at least one bonding wire extends at an angle other than 90 degrees from edge 846 of interposer 836. Interposer 836 is shown in plan view in Fig. 12 as being rectangular in shape. By ordinary principles of geometry, a wire which is not perpendicular to one edge of a rectangular interposer 836 is not perpendicular to any other edge of the same interposer. The bonding wires illustrated in Fig. 13, therefore, are oriented "at an angle substantially less than 90 degrees from any side of the section of interposer . . .," as recited in claim 6. The same recitation in claims 12 and 17 is applied to the disclosure in exactly the same manner.

Applicant has reviewed the claims but has not found any additional deficiencies in application of the claims to the disclosure.

OTHER REQUIREMENTS -

The Official Action also states that "applicant has otherwise failed to fully comply with the requirements of 37 C.F.R § 1.607(2), (3), (5) and (6)." This statement is understood by applicant as requiring further action to comply with these requirements.

37 CFR 1.607(a)(2)

With respect to the requirement of 37 CFR § 1.607(2), for a proposed count, applicant hereby proposes the following counts I and II:

Proposed Count I

1. A method of assembling a plurality of semiconductor chips, comprising the steps of:

(a) providing a portion of a semiconductor wafer containing the plurality of chips thereon, each

of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;

(b) assembling a respective section of a dielectric interposer to each respective one of the plurality of chips individually, without detaching the plurality of chips from the portion of the semiconductor wafer, each section of interposer having a plurality of bonding pads near an outer periphery of the section, such that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips;

(c) wire bonding each bonding pad to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips;

(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and

(e) cutting the encapsulated chips from the semiconductor wafer.

Proposed count I is verbatim identical to claim 1 of the '070 patent and to claim 1 of the present application.

Proposed Count II

1. A method of assembling a plurality of semiconductor chips, comprising the steps of:

(a) providing a portion of a semiconductor wafer containing the plurality of chips thereon, each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;

(b) assembling a respective section of a dielectric interposer to each respective one of the

plurality of chips individually, without detaching the plurality of chips from the portion of the semiconductor wafer, each section of interposer having a plurality of bonding pads near an outer periphery of the section, such that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips;

(c) wire bonding each bonding pad to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips;

(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and

(e) cutting the encapsulated chips from the semiconductor wafer,

wherein step (b) includes providing an elastomer between each of the plurality of chips and the respective interposer on the chip.

Proposed Count II is identical to claim 6 of the '070 patent and identical to claim 3 of the present application, in each case rephrased as an independent claim incorporating all of the recitations in the base claim.

37 CFR 1.607(a)(3)

With respect to the 37 CFR § 1.607(3), applicants identify the following claims of the '070 patent as corresponding to count I: 1-15 inclusive.

Applicants identify the following claims of the '070 patent as corresponding to proposed count II: 6 and 13.

37 CFR 1.607(a)(4)

With respect to 37 CFR § 1.607(4), applicants have already presented claims in the present application corresponding to the proposed counts. Applicants identify the

following claims of the present application as corresponding to proposed count I: 1, 2, 4-6 inclusive; 18 and 19; and 21-23 inclusive. Applicants identify the following claims in the present application as corresponding to proposed count II: 3 and 20.

REASONS WHY APPLICATION CLAIMS CORRESPOND TO THE COUNTS

Application claim 1 corresponds exactly to proposed count I.

Application claim 2 differs from proposed count I only in that application claim 2 requires that the wire bonding process to a bonding pad include either micro-resistant welding or ultrasonic bonding. "Ultrasonic wire bonding is known for purposes of attaching wire interconnections to semiconductor devices . . ." *Smith et al.*, U.S. Patent 4,976,392,[1] col. 1, lns. 8-10. Additionally, micro-resistant welding is an old technique for bonding wires to semiconductor chips and to packaging substrates, as taught, for example, in *Funari*, U.S. Patent 4,171,477. Indeed, *Funari* '477 (col. 8, lns. 51, *et seq.*) demonstrates that both micro-resistant wire bonding and ultrasonic bonding were regarded by the art as interchangeable, art-recognized alternatives for performing a wire bonding operation. Application claim 2 encompasses subject matter which would be obvious over proposed count I. Accordingly, claim 2 corresponds to proposed count I.

Application claim 3 is verbatim identical to proposed count II except that claim 3 of the application is phrased as a dependent claim, whereas proposed count II is written as an independent claim.

[1] An Information Disclosure Statement submitted herewith makes of record all references referred to herein which were not previously of record.

Application claim 4 differs from proposed count I only in that the "portion of the semiconductor wafer" which is already specified in count I as being "a portion of a semiconductor wafer containing the plurality of chips" is specified in claim 4 as being "the whole semiconductor wafer." Manifestly, given the teaching to use some portion of a semiconductor wafer, it would be obvious to use a larger portion of the wafer or a smaller portion including a larger or smaller number of chips. Such a change constitutes a mere change in the size of the "portion."

Application claim 5 differs from proposed count I only in that claim 5 requires ultrasonic bonding at both ends of each wire. As previously pointed out, ultrasonic bonding is and was a common, well-known method of wire bonding.

Application claim 6 differs from proposed count I only in that application claim 6 requires placement of a bonding wire at an angle other than perpendicular to "any side of the section of interposer having the bonding pad to which the one wire is bonded," *i.e.*, wire bonding at an angle other than perpendicular to the edge of the dielectric element bearing the bonding pad. *Hill et al.*, U.S. Patent 5,091,825, specifically illustrates (*e.g.*, Fig. 2) a commonplace arrangement in which a substrate 52 bears a row of bond pads 58 and the chip 50 bears a similar row of bond pads 54a, 54b, 54c, etc., at a different spacing than pads 58a, 58b and 58c. Wire bonds 56a, 56b and 56c extend, as they must, at an acute angle to an edge 66 of the chip and also at an acute angle to the edge of substrate 52 (the horizontal edge adjacent the row of bond pads 58a, 58b and 58c). In the structure of *Hill et al.*, the angular arrangement is "inherent" and required in at least some bonding wires because the length of a row of bond pads on the substrate is different from the length of a row of bond pads on the chip. See col. 1, lns. 15-

29. It would be obvious to adopt this arrangement in the method of count I, for the same reasons, and adopting this arrangement would result in the method of claim 6. As further shown, for example, by, *e.g.*, *Kilby*, U.S. Patent 3,643,138 (*e.g.*, Fig. 8) and *Sinnaduri et al.*, U.S. Patent 4,448,306 (Fig. 1 and col. 2, lns. 16-19), it is commonplace in the art to place wire bonds at random orientations relative to the edges of the chip and, hence, at random orientations relative to the edges of an associated dielectric element in order to make the required connections between the contacts of the chip and the bonding pads of the dielectric element. For all of these reasons, application claim 6 represents an obvious variant of count I and corresponds to the count.

Claims 18-34 are essentially identical to claims 1-17, except that claims 18-34 were rephrased to overcome rejections under 35 U.S.C. § 112 and, thus, clarify the meaning of certain passages in the claims. An exhibit showing the differences between claims 18-34 and claims 1-17 was made of record with applicant's Amendment dated June 7, 2001. Claims 18, 19 and 21-23 are identical to claims 1,2 and 4-6 with certain limitations in claims 18, 19 and 23 rephrased for greater clarity, but without substantive change. Thus, the correspondence between application claims 18, 19 and 21-23 correspond to proposed count I for the same reasons as application claims 1,2 and 4-6, respectively. Likewise, application claim 20 is the same as application claim 3 but for the dependence of claim 20 on claim 18 (modified claim 1). Claim 20 corresponds to proposed count II for the same reasons as claim 3.

REASONS WHY PATENT CLAIMS CORRESPOND TO THE COUNT

Claim 1 of the '070 patent corresponds exactly to proposed count I.

'070 patent claim 2 differs from proposed count I only in that claim 2 requires that the step of bonding an end of each wire to a "respective bonding pad," *i.e.*, a bonding pad of the dielectric interposer, be performed either by micro-resistant welding or by ultrasonic bonding. Ultrasonic wire bonding is a well-known, commonplace method of wire bonding, as shown, for example, by *Smith et al.* '392, column 1, lines 8-10. That, alone, would be enough to render the species of claim 2 obvious over the genus of count I. Moreover, micro-resistant welding is also a well-known, obvious alternative for performing the wire bonding process, as taught, for example, by *Funari* '477. Indeed, *Funari* '477 (col. 8, lns. 51, *et seq.*) demonstrates that both micro-resistant wire bonding and ultrasonic bonding were regarded by the art as interchangeable, art-recognized alternatives for performing a wire bonding operation. Accordingly, '070 claim 2 would be obvious over proposed count I and corresponds to the count.

'070 claim 3 merely adds further specificity to the choice of art-recognized alternatives, in that it bonds one end of the wire with micro-resistant welding and another using ultrasonic bonding. Mere selection of art-recognized methods for performing the same steps specified in step (c) of proposed count I does not patentably distinguish the claim from the count and, hence, the claim corresponds to the count.

'070 claim 4 merely specifies the use of "a dual electrode bonding tool to perform micro-resistant welding." That is the conventional way of performing micro-resistant welding in a wire bonding operation, as taught in *Funari* '477 ("a pair of juxtaposed electrically conducting bonding tip members 10 and 11 which are electrically isolated from one another . . . ;" *see* also, the "bonding tips 51, 52" shown in Fig. 6 and described at col. 9, lns. 10, *et seq.*).

'070 claim 5 adds to claim 1 the steps of testing the chips "on the portion of the semiconductor wafer" and rejecting bad chips, *i.e.*, "determining whether" each chip meets "acceptance criteria" and selecting "only those chips which comply with the acceptance criteria" for further processing. The notion of testing a wafer and excluding bad chips from further processing is the conventional practice in the art, as shown, for example, by *Kunieda et al.*, U.S. Patent 4,921,810, which explains (background section) that wafers are tested and the "circuits which have failed the test are discarded, while the circuits which have passed the test are placed in packages . . ." Application of the common wisdom in the art -- that one does not waste money packaging bad chips -- in the context of proposed count I would lead directly to the alleged invention of '070 claim 5. Accordingly, claim 5 is obvious over count I and corresponds to the count.

'070 patent claim 6 corresponds exactly to proposed count II. Moreover, '070 patent claim 6 also corresponds substantially to proposed count I. In this respect, '070 patent claim 6 differs from verbatim identical claim 3 of the present application. The '070 patent has an earliest alleged effective filing date of May 15, 1997. Prior art available against the claims of the '070 patent, including PCT published international application WO 92/05582, discloses the use of an elastomer layer between the interposers and chips in the system of proposed count I, and thus renders '070 patent claim 6 obvious over proposed count I. The specification of the WO 92/05582 publication is identical to the specification of the present application as filed. The passages of the present application cited in applying application claim 3 to the present disclosure offer the relevant teachings. See, *e.g.*, page 5, line 34-page 6, line 2 page 32, line 36 to page 33, line 3 and page 41, lines

15-35 and page 19, lines 14-16 as well as Figs. 9 and 13 in the WO 92/05582 publication for discussion of elastomer layers. This disclosure is not available as prior art against the claims in the present application, and accordingly does not cause claim 3 of the present application to correspond to proposed count I.

'070 patent claim 7 differs from proposed count I in that patent claim 7 recites that the "portion of the semiconductor wafer" includes "the whole semiconductor wafer." Given the teaching, to use a portion of a semiconductor wafer which includes a plurality of chips, it would be obvious to use a larger portion of the wafer including a larger plurality of chips, up to and including the whole wafer. Such a change constitutes a mere change in the size of the "portion" treated. Accordingly, claim 7 corresponds to proposed count I.

'070 patent claim 8 differs from proposed count I only in that it recites the use of ultrasonic bonding at both ends of each wire. As pointed out above, ultrasonic bonding is a conventional method of wire bonding, and among the art-recognized alternatives for performing the task of wire bonding specifically called out in proposed count I. *See Smith et al.* '392.

'070 claim 9 adds to proposed count I the step of detecting defective wire bonds and repairing the same by removing the defectively-bonded wire and wire bonding a new wire in its place (between steps (c) and (d), *i.e.*, after the initial wire bonding step of proposed count I and before encapsulating the wires). Like any other manufactured product, wire bonds commonly are subjected to inspection during manufacture. As described, for example, in the background section of *Shibasaka et al.* U.S. Patent 5,156,319 (col. 1, lns. 11-20) it has been the common practice in the industry to inspect wire bonds in a

wire-bonded semiconductor chip assembly, remove the defective wire bonds and replace the same prior to encapsulation or "sealing". If one intends to repair the assembly by replacing defective wire bonds, rather than discard the entire assembly, the defect-detection and repair operation can only be performed after the wire bonds are made but before the same are covered with an encapsulant, *i.e.*, between steps C and D of proposed count I as recited in '070 claim 9. Thus, claim '070 9 represents an obvious variant of proposed count I.

Claim 10 of the '070 patent differs from proposed count I only in that it recites orienting a bonding wire "at an angle less substantially less than 90° from any side of the section of interposer . . ." As explained above, at most this recitation requires placement of a bonding wire at an angle other than perpendicular to an edge of the interposer. *Hill et al.*, U.S. Patent 5,091,825, specifically illustrates (*e.g.*, Fig. 2) a commonplace arrangement in which a substrate 52 bears a row of bond pads 58 and the chip 50 bears a similar row of bond pads 54a, 54b, 54c, etc., at a different spacing than pads 58a, 58b and 58c. Wire bonds 56a, 56b and 56c extend, as they must, at an acute angle to an edge 66 of the chip and also at an acute angle to the edge of substrate 52 (the horizontal edge adjacent the row of bond pads 58a, 58b and 58c). In the structure of *Hill et al.*, the angular arrangement is required in at least some bonding wires because the length of a row of bond pads on the substrate is different from the length of a row of bond pads on the chip. See column 1, lines 15-29. It would be obvious to adopt this arrangement in the method of count I, for the same reasons, and adopting this arrangement would result in the method of claim 6. As further shown, for example, by, *e.g.*, *Kilby*, U.S. Patent 3,643,138 (*e.g.*, Fig. 8) and *Sinnaduri et al.*, U.S. Patent 4,448,306 (Fig. 1 and col. 2, lns. 16-19), it

is commonplace in the art to place wire bonds at random orientations relative to the edges of the chip and, hence, at random orientations relative to the edges of an associated dielectric element in order to make the required connections between the contacts of the chip and the bonding pads of the dielectric element. Thus, '070 claim 10 corresponds to proposed count I.

Claim 11 of the '070 patent differs from proposed count I only in that the claim recites the use of "a semiconductor chip," i.e., a portion of a semiconductor wafer containing only one chip rather than a portion including "plurality of chips" recited in proposed count I and consequently omits the step of "cutting" the chips apart as recited in proposed count I. Here again, varying the number of chips including in a portion of a wafer does not patentably distinguish the claim from the proposed count. Moreover, WO 92/05582, available as a reference against the '070 claims, explicitly teaches the alternatives of assembling the interposers either to individual chips (*e.g.*, pp. 14-30 and 32-49) or to a multi-chip unit such as a wafer (*e.g.*, pp. 31-32). Application of this recognized alternative in proposed count I suggests '070 claim 11. '070 claim 11 also recites bonding one end of each wire using microresistant welding and the opposite end using ultrasonic bonding. As explained above, both of these expedients are well known, art-recognized alternatives for performing the wire bonding step of proposed count I, step (c). See *Smith et al.*, U.S. Patent 4,976,392 and *Funari*, U.S. Patent 4,171,477, both of which are discussed above. Selection of known, art-recognized alternatives for bonding a wire also does not patentably distinguish claim 11 over proposed count I.

'070 claim 12 adds the further recitation of using a "dual electrode bonding tool," the precise method taught by

Funari '477 as explained above in connection with claim 4. Thus, claim 12 also corresponds to proposed count I.

Claim 13 of the '070 patent corresponds to proposed count II. The differences between claim 13 and proposed count II are the same as the differences addressed above between claim 11 and proposed count I, i.e., the use of a smaller wafer portion, containing only a single chip, and the use of the conventional ultrasonic and micro-resistant welding steps to perform the wire-bonding operation. For the same reasons, claim 13 does not patentably distinguish over proposed count II. Also, for substantially the same reasons as discussed above in connection with '070 claim 6, '070 claim 13 additionally corresponds to proposed count I. Again, given the prior art available against the claims of the '070 patent, including WO 92/05582, which specifically discloses the use of the elastomer as recited in '070 claim 13, addition of the elastomer limitation does not distinguish the claim over proposed count I.

'070 claim 14 recites the same testing and repair steps as discussed above in connection with '070 claim 9. For the same reasons as discussed in connection with claim 9, these steps do not patentably distinguish '070 claim 14 over proposed count I, and accordingly this claim corresponds to proposed count I.

'070 claim 15 includes the same recitation as the orientation of the bonding wires at an angle other than perpendicular to the side of the "section of interposer." As discussed above in connection with claim 10, these steps do not patentably distinguish the claim over proposed count I.

37 CFR § 1.607(a)(5)

The terms of the present application claims have been addressed and applied to the disclosure of the application in

applicants' last previous amendment and in the further discussion above responsive to the Examiner's holding that certain claims had not been fully applied to the disclosure.

37 CFR § 1.607(a)(6)

Claims 1-17 inclusive were original claims of the present application, and were present in the application within one year after the issue date of the '070 patent. Accordingly, 35 U.S.C. § 135(b) has been met with respect to those claims.

As set forth above, claims 18-34, added by amendment more than one year after the issue date of the '070 patent are replicates of claims 1-17 with clarifications of certain features in response to a previous § 112, second paragraph rejection of claims 1-17. As is believed clear from Exhibit A attached to applicant's last previous amendment, none of these changes added or removed any material limitation from the previously presented claims. For example, claim 18 differs from originally presented claim 1 only in that claim 18 includes a "whereby" clause stating the inevitable result of wire bonding namely, the presence of "wires." This change merely provides antecedent basis for a feature in dependent claim 19. That claim differs from original claim 2 in that claim 19 refers to "one end of each one of said wires" instead of "one end of each wire." Here again, the only difference between claim 19 and originally presented claim 2 is that claim 19 states the same limitations in clearer terms. Claims 20-22 are identical to the originally presented dependent claims 3-5, but for the inconsequential change to independent claim 18. Claim 23 restates the identical features previously stated, in obscure terms, in originally presented dependent claim 6. As explained above, the original recitation that a wire is oriented at an angle "substantially less than 90° from any side" of a section of

the interposer means that the wire bond is oriented at an angle other than 90° from any edge of the interposer. Here again, rephrasing does not add or delete any material limitation from the originally presented dependent claim 6. The changes to claims 24, 25, 29, 30, 31 and 34, vis-a-vis originally presented claims 7, 8, 12, 13, 14 and 17, respectively, are the same.

In considering whether claims presented more than one year after the issue date of the patent comply with 35 U.S.C. § 135(b), the issue is not whether the identical language was used in a claim presented less than one year after the issue date but rather whether any claims in the application prior to the one year date "includes all the material limitations of" the later presented claim, *e.g.*, *Pizzurro v. Phund*, 1 U.S.P.Q.2d 1056, 1061 (BPAI, 1984). If the process steps recited in the later-presented claim are inherent in the earlier-presented claim, the two claims are substantially the same for purposes of 35 U.S.C. § 135(b). *Corbett v. Chisholm*, 496 U.S.P.Q. 337, 342-3 (CCPA 1977). Here, the steps of each of claims 18-34 manifestly are inherent in a corresponding ones of earlier-presented claims 1-17. Accordingly, 35 U.S.C. § 135(b) is met.

Favorable reconsideration and declaration of an interference between the present application and U.S. Patent 5,950,070 are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any charges in connection with this response, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: April 4, 2002

Respectfully submitted,

By_____

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